

ABSTRACT

An existent DRAM memory cell comprises transistors as a switch and capacitors for accumulating storage charges in which the height of the capacitor has been increased more and more along with micro miniaturization, which directly leads to increase in the manufacturing cost. The invention of the present application provides a semiconductor memory device of a basic constitution in which a memory cell array having plural memory cells disposed on a semiconductor substrate and word lines and data lines for selecting the memory cells and a peripheral circuit at the periphery of the memory cell array wherein the memory cell comprises a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and a potential can be applied to the insulating layer enabling the tunneling effect. The invention of the present application concerns a memory cell not requiring capacitor and capable of being formed in simple steps.

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